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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,400	02/17/2004	Naoki Mizoguchi	36856.1204	1616

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KEATING & BENNETT, LLP
10400 EATON PLACE
SUITE 312
FAIRFAX, VA 22030

EXAMINER	
HAM, SEUNGSOOK	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 03/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/780,400	MIZOGUCHI ET AL.	
	Examiner	Art Unit	
	Seungsook Ham	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 11* is/are rejected.

7)☒ Claim(s) *10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/25/04, 2/17/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the subject matter of claim 6 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 5, 6, 8, and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Mizoguchi et al. (JP 2002-325002 or JP 2002-335111).

Mizoguchi et al. (JP '002, figs. 1(a)-2(b), 6(a), 6(b)) discloses an electronic chip comprising: a resonator electrode 9 provided in the chip; input and output electrodes 5, 6 extending in a vertical direction of the chip through via-hole electrodes 7, 8, which are coupled to the resonator electrode; a first ground electrode 3, 4 disposed around the chip and having a tubular shape so as to enclose the resonator electrode; the input and output electrodes are disposed at inner sides of the tubular first ground electrode such that the input and output electrodes are not electrically connected to the first ground electrode; at least a pair of second ground electrodes 10, 11 which are disposed on both sides of at least one of the input and output electrodes and which are electrically connected to the first ground electrode; the second ground electrodes electrically connected to the first ground electrode at least one of the upper surface and the lower surface of the chip 2a, 2b; and the resonator electrode generates a plurality of resonance modes (i.e. dual-mode) and includes a through hole 9a.

Mizoguchi et al. (JP '111, figs. 1-4) discloses an electronic chip comprising: a resonator electrode 23 provided in the chip; input and output electrodes 31, 32

extending in a vertical direction of the chip through via-hole electrodes 34a, 34b, which are coupled to the resonator electrode; a first ground electrode 33, 38 disposed around the chip and having a tubular shape so as to enclose the resonator electrode; the input and output electrodes are disposed at inner sides of the tubular first ground electrode such that the input and output electrodes are not electrically connected to the first ground electrode; at least a pair of second ground electrodes 3 which are disposed on both sides of at least one of the input and output electrodes and which are electrically connected to the first ground electrode; the second ground electrodes electrically connected to the first ground electrode at least one of the upper surface and the lower surface of the chip 33, 38 and the resonator electrode generates a plurality of resonance modes (i.e. dual-mode) and includes a through hole 23a.

Claims 1, 2, 4, 5, 7-9 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Kaminami et al. (JP 2002-280806).

Kaminami et al. (figs. 1(a)-6(b)) discloses an electronic chip comprising: a ring-shape resonator electrode 9 provided in the chip; input and output electrodes 4, 5 extending in a vertical direction of the chip, which are coupled to the resonator electrode; a first ground electrode 3, 6, 7, 8 disposed around the chip and having a tubular shape so as to enclose the resonator electrode; the input and output electrodes 4, 5 are disposed at inner sides 10, 11 of the tubular first ground electrode such that the input and output electrodes are not electrically connected to the first ground electrode; at least a pair of second ground electrodes 41, 42 which are disposed on both sides of at least one of the input and output electrodes and which are electrically connected to

the first ground electrode (see fig. 6(a)); the second ground electrodes electrically connected to the first ground electrode at least one of the upper surface and the lower surface of the chip 3, 6 and the resonator electrode generates a plurality of resonance modes (i.e. dual-mode) and includes a through hole 9a.

Claims 1, 2, 5, 8, 9 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Kaminami et al. (JP 2002-368503).

Kaminami et al. (figs. 1(a), 1(b)) discloses an electronic chip comprising: a ring-shape resonator electrode 5 provided in the chip; input and output electrodes 6, 7 extending in a vertical direction of the chip, which are coupled to the resonator electrode; a first ground electrode 3, 4 disposed around the chip and having a tubular shape so as to enclose the resonator electrode; the input and output electrodes are disposed at end portions 2c, 2d of the tubular first ground electrode such that the input and output electrodes are not electrically connected to the first ground electrode; at least a pair of second ground electrodes 8, 9 which are disposed on both sides of at least one of the input and output electrodes and which are electrically connected to the first ground electrode; the second ground electrodes electrically connected to the first ground electrode at least one of the upper surface and the lower surface of the chip 3, 4 and the resonator electrode generates a plurality of resonance modes (i.e. dual-mode) and includes a through hole 5a.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kaminami et al. (JP 2002-280806 or JP 2002-368503) or Mizoguchi et al. (JP 2002-325002 or JP 2002-335111) in view of Kanba et al. (US Apt. Appl. Publ. '960).

Kaminami et al. or Mizoguchi et al. does not show the first ground electrode being embedded in the chip. However, such design technique is well known in the art. Kanba et al. (fig. 1C) discloses a similar chip resonator having the first ground electrode embedded in the chip. It would have been obvious to place the first ground electrode embedded in the chip in the device of kaminami et al. or Mizoguchi et al. since such design technique is well known in the art, and such modification does not alter the chip characteristics as shown by Kanba et al.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kaminami et al. (JP 2002-280806 or JP 2002-368503) in view of Mizoguchi et al. (JP 2002-325002).

Kaminami et al. are applied as above. Both references do not show the input and output electrodes include via-hole electrode to led to the upper of lower surface of the chip. However, such design technique is well known in the art. Mizoguchi et al. (fig. 1(a)) discloses input and output electrodes 5, 6 include via-holes 7, 8 electrodes to extend and led to the upper surface of the chip.

It would have been obvious to one of ordinary skill in the art to use via-hole electrodes to led the input and output electrodes to the upper surface of the chip in the

device of Kaminami et al. since such design technique is well known in the art as shown by Mizoguchi et al.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mizoguchi et al. (JP 2002-325002 or JP 2002-335111).

Providing a ring-shaped resonator is considered as an obvious modification since such resonator is well known in the art, and it requires only a routine skill in the art.

Claims 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizoguchi et al. (JP 2002-325002 or JP 2002-335111) or Kaminami et al. (JP 2002-368503) in view of Kaminami et al. (JP 2002-280806).

Mizoguchi et al. and Kaminami et al. (JP '503) are silent as to whether the first ground electrodes is disposed on the pair of side surfaces of the chip, and the second ground electrodes extend in the vertical direction at the end surfaces of the chip. However, such design techniques are well known in the art as shown by Kaminami et al. (JP '806, figs.1(a) and 6(a)). Therefore, it would have been obvious to one of ordinary skill in the art to provide the first ground electrodes on the side surfaces of the chip or the second ground electrodes on the end surface of the chip in the device of Mizoguchi et al. or Kaminami et al. (JP '503) since such modification does not alter the device characteristics and also well known in the art as shown by Kaminami et al. (JP '806).

Allowable Subject Matter

Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Estes et al. and Shapiro disclose a filter having via-hole ground electrodes to suppress unwanted signals.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Seungsook Ham whose telephone number is (571) 272-2405. The examiner can normally be reached on Monday-Thursday, 8:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571)-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Seungsook Ham
Primary Examiner
Art Unit 2817

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